
# Aim High
## HPC @ Intel

CAS2K7 Workshop
September 10, 2007

Stephen R. Wheat, Ph.D.
Director, HPC
Digital Enterprise Group

# Risk Factors

Today's presentations contain forward-looking statements. All statements made that are not historical facts are subject to a number of risks and uncertainties, and actual results may differ materially. Please refer to our most recent Earnings Release and our most recent Form 10-Q or 10-K filing available on our website for more information on the risk factors that could cause actual results to differ.

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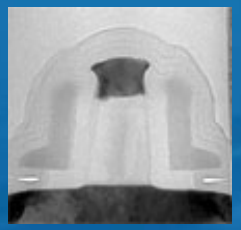
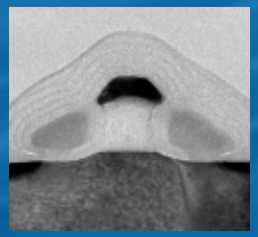
Rev. 7/19/06

# Silicon Future

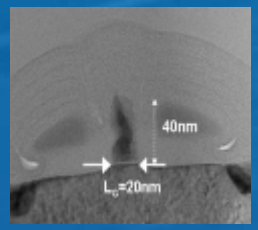
90nm
2003



65nm
2005

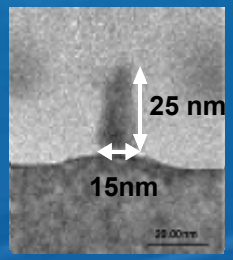


45nm
2007

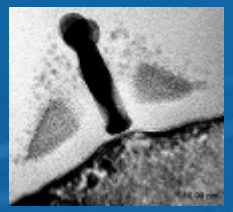



2005 – 2012

32nm
2009




22nm
2011



2013 – 2017

16nm
2013

11nm
2015

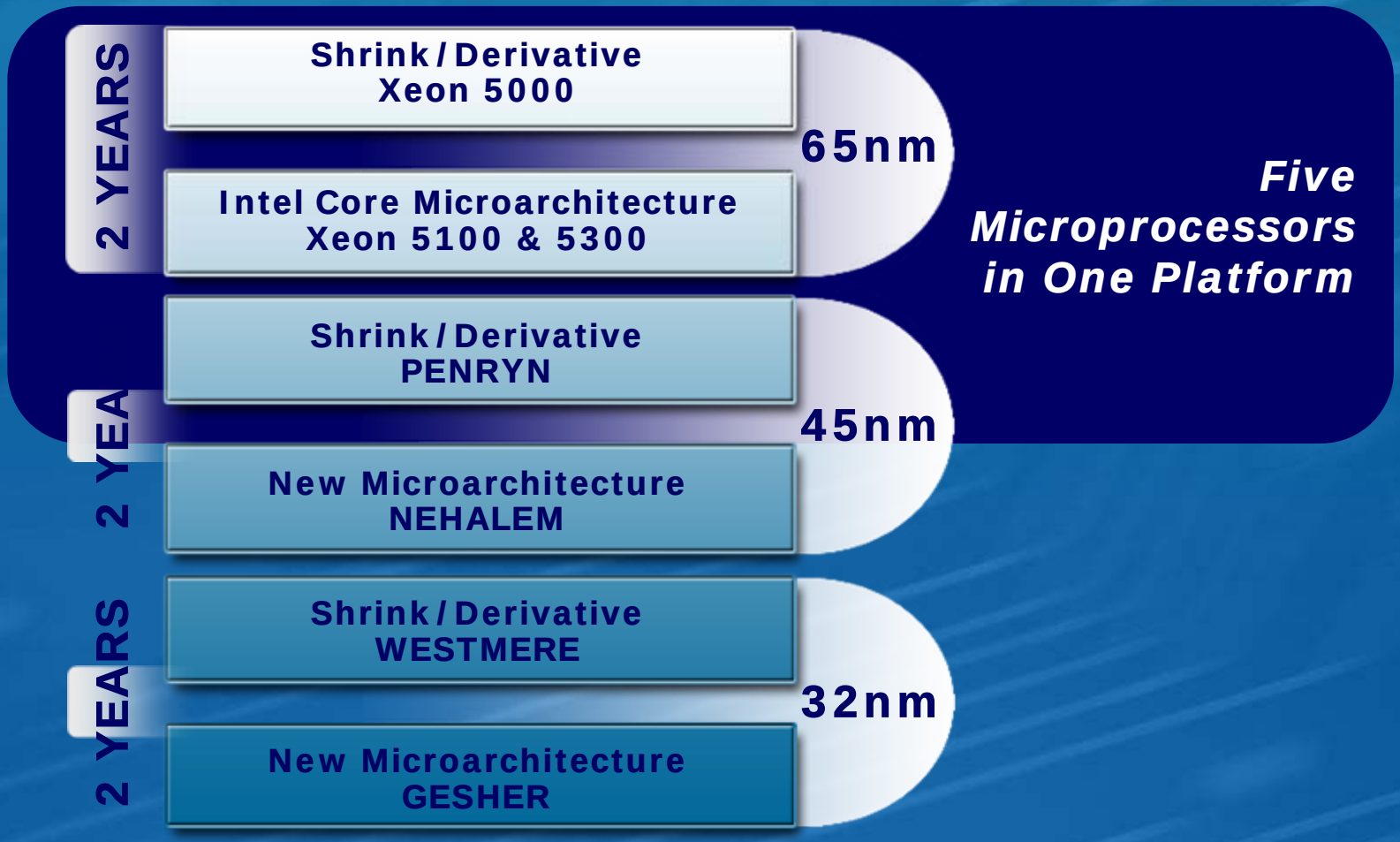
8nm
2017

New Intel technology generation every 2 years
Intel R&D technologies drive this pace well into the next decade

Roadmap

Research

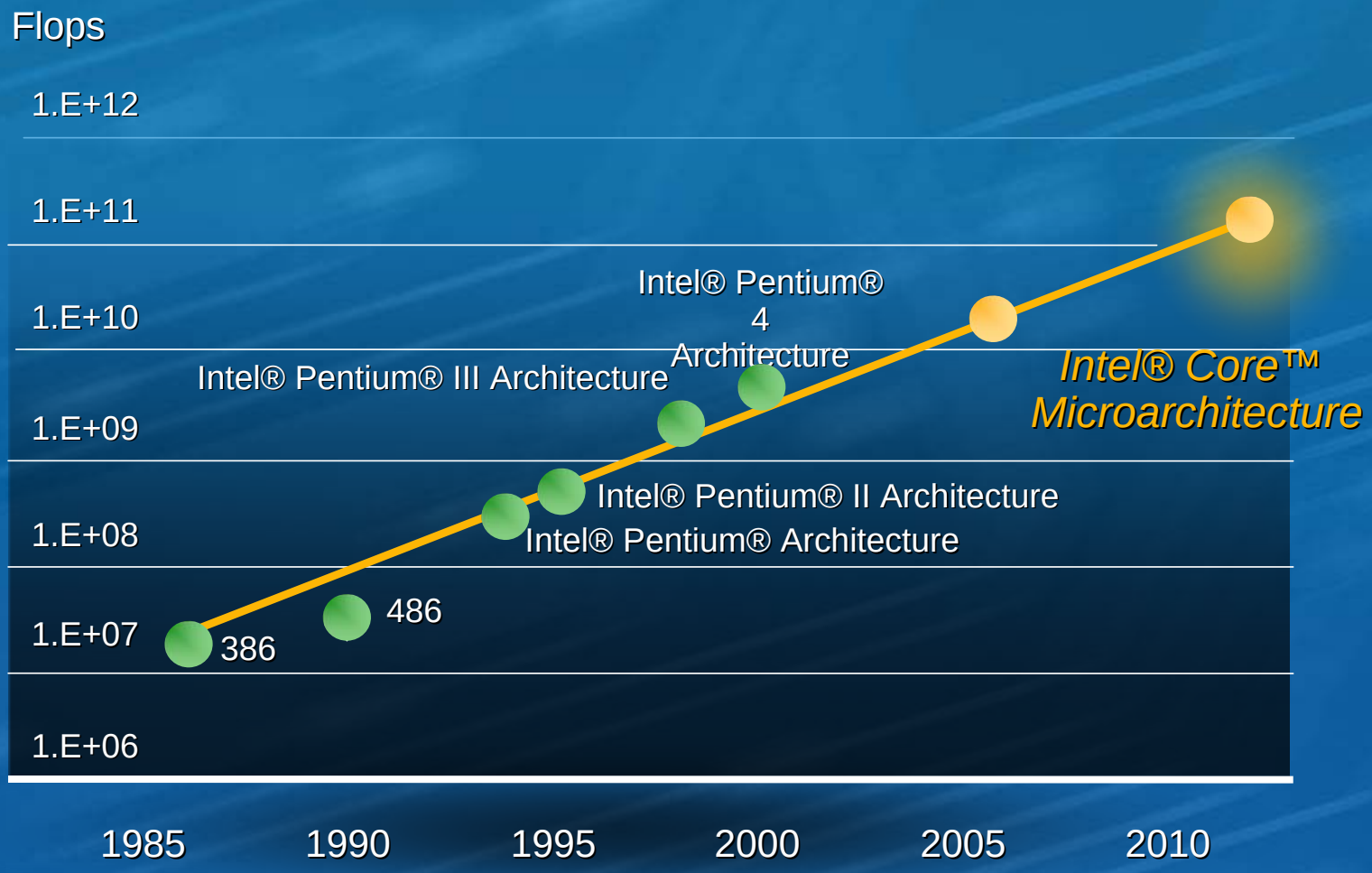
# Intel Design & Process Cadence



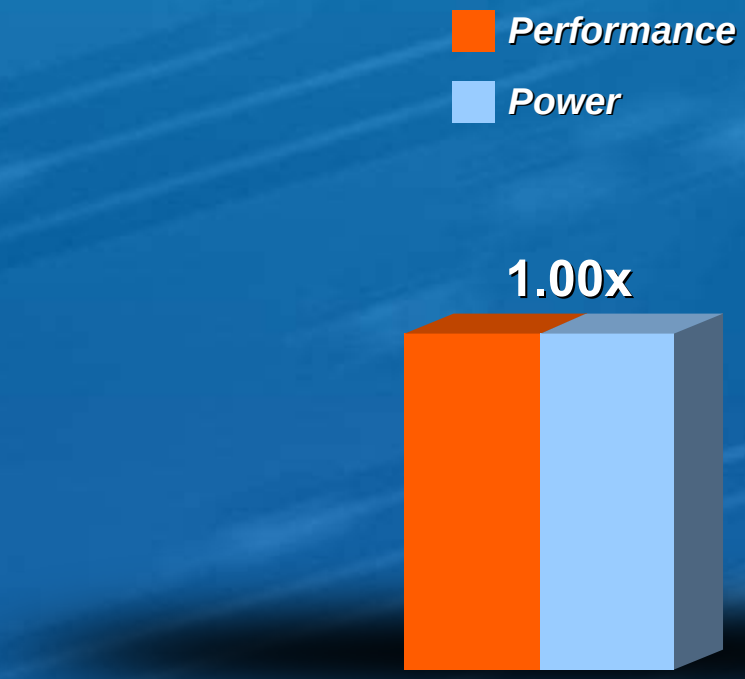



All dates, product descriptions, availability and plans are forecasts and subject to change without notice.

# Processor Performance

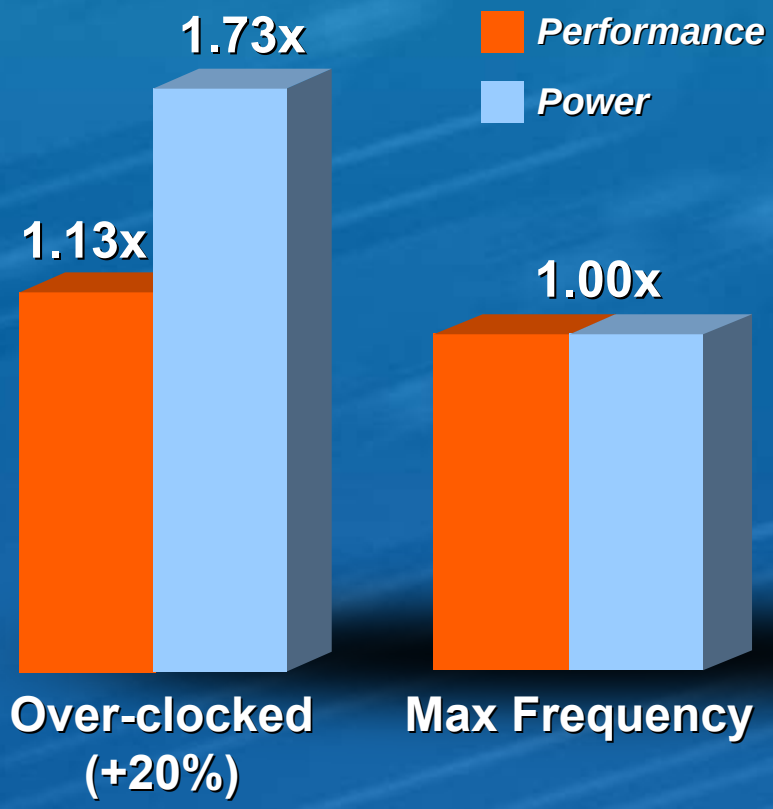


# Why Multi-Core?



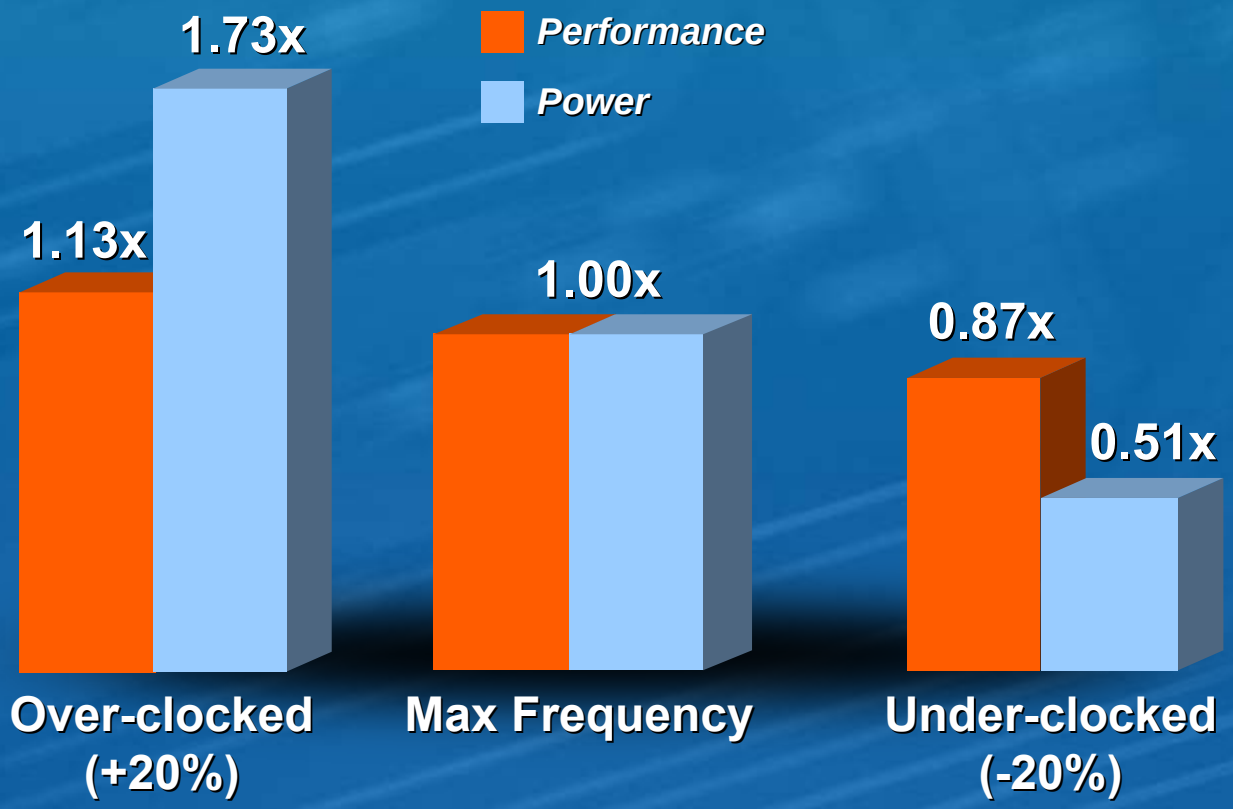

*Relative single-core frequency and Vcc*

# Over-clocking



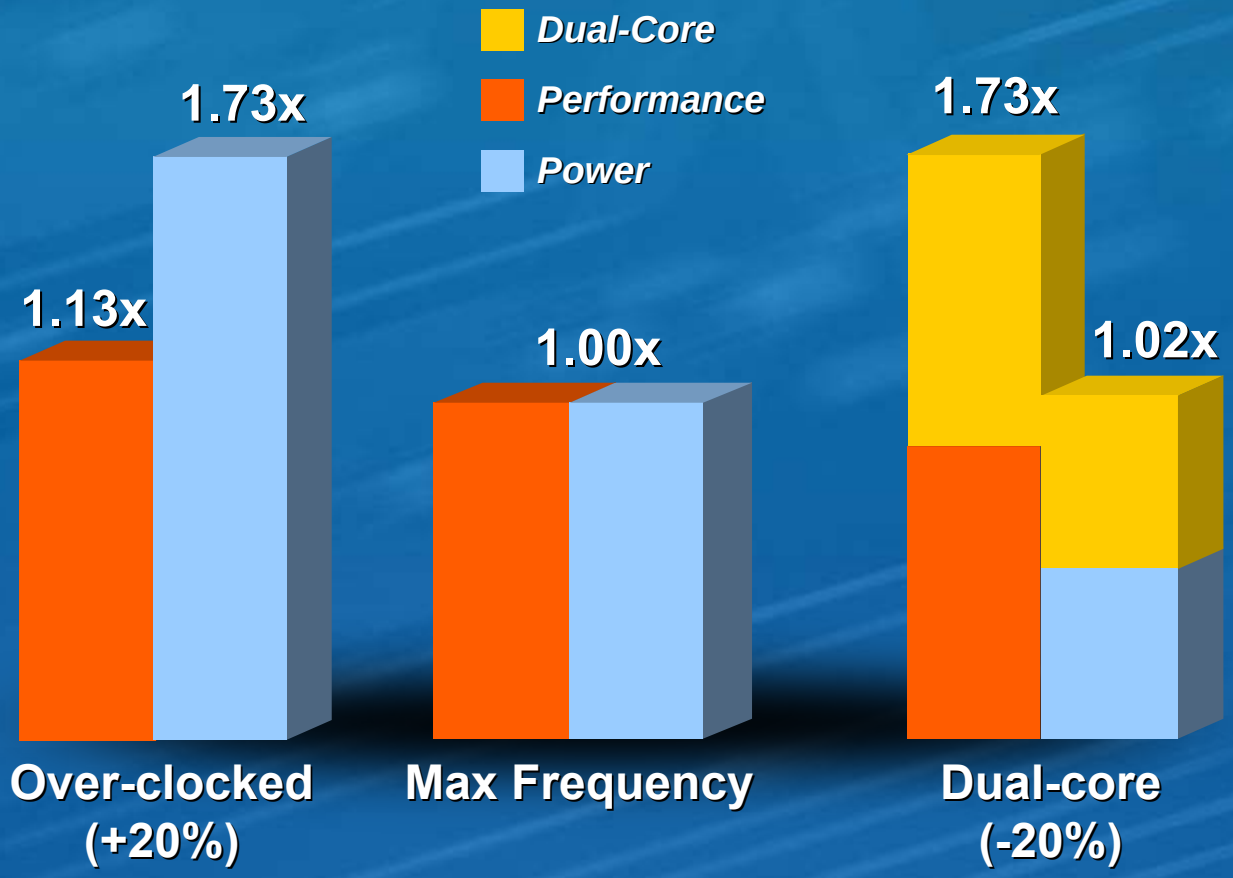

*Relative single-core frequency and Vcc*

# Under-clocking




*Relative single-core frequency and Vcc*

# Multi-Core
# Energy-Efficient Performance




*Relative single-core frequency and Vcc*

# Multi-threaded Cores

*All Large Core*

*Mixed Large and Small Core*

*All Small Core*

*Goal: Energy Efficient Petascale with Multi-threaded Cores*

Note: the above pictures don't represent any current or future Intel products

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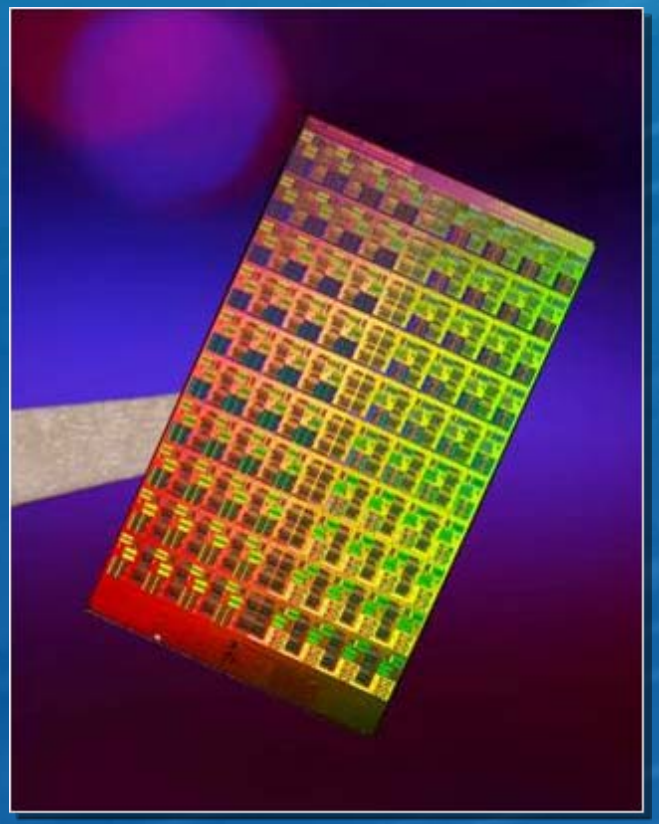
# Teraflops Research Chip

**100 Million Transistors • 80 Tiles • 275mm²**



First tera-scale programmable silicon:

- Teraflops performance
- Tile design approach
- On-die mesh network
- Novel clocking
- Power-aware capability
- Supports 3D-memory

Not designed for IA or product

# Tera-scale Introduction

- Represents significant Intel transition from “large” cores to 32+ low-power, highly-threaded IA cores per die
- Motivations for a new architecture
  - Enable emerging workloads and new use-models
  - Low Power IA cores provide 4-5X greater performance-power efficiency
  - Scaling beyond the limits of Instruction level parallelism and single-core power
- Tera-scale is *NOT* simply SMP-on-die
  - Will require complete platform and software enabling

| Parameter | SMP | Tera-scale | Improvement | Optimizations |
|---|---|---|---|---|
| Bandwidth | 12 GB/s | ~1.2 TB/s | ~100X | Massive bandwidth between cores |
| Latency | 400 cycles | 20 cycles | ~20X | Ultra-fast synchronization |

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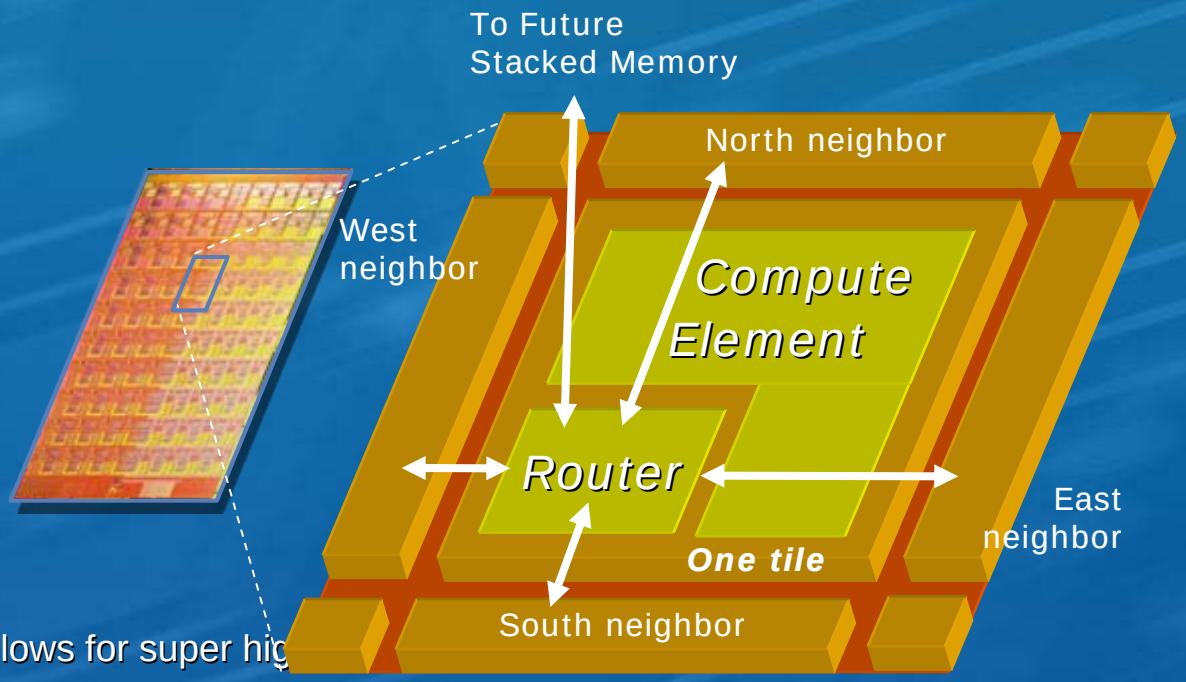
# Tiled Design & Mesh Network

**Repeated Tile Method:**

- Compute + router
- Modular, scalable
- Small design teams
- Short design cycle




**Mesh Interconnect:**

- "Network-on-a-Chip"
  - Cores networked in a grid allows for super hig
    communications in and between cores
- 5-port, 80GB/s* routers
- Low latency (1.25ns*)
- Future: connect IA/or and special purpose cores

* When operating at a nominal speed of 4GHz

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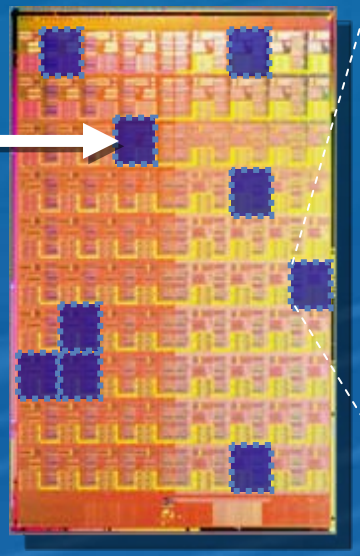
# Fine Grain Power Management

- Novel, modular clocking scheme saves power over global clock
- New instructions to make any core sleep or wake as apps demand
- Chip Voltage & freq. control (0.7-1.3V, 0-5.8GHz)

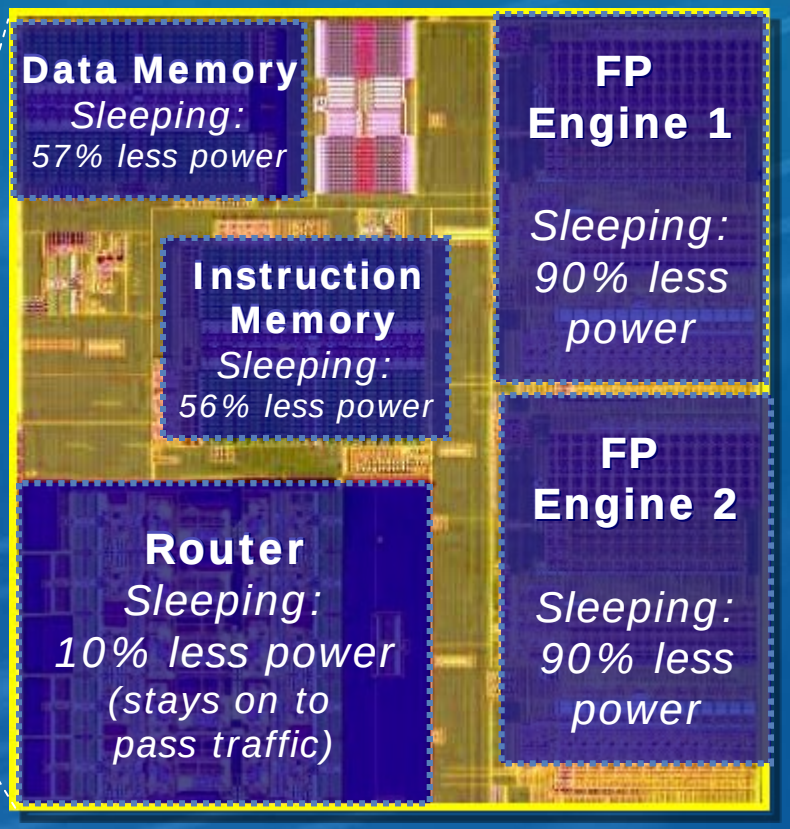
**Dynamic sleep**

**STANDBY:**
- Memory retains data
- **50%** less power/tile

**FULL SLEEP:**
- Memories fully off
- **80%** less power/tile



***21 sleep regions per tile*** *(not all shown)*




**Industry leading energy-efficiency of 16 Gigaflops / Watt**

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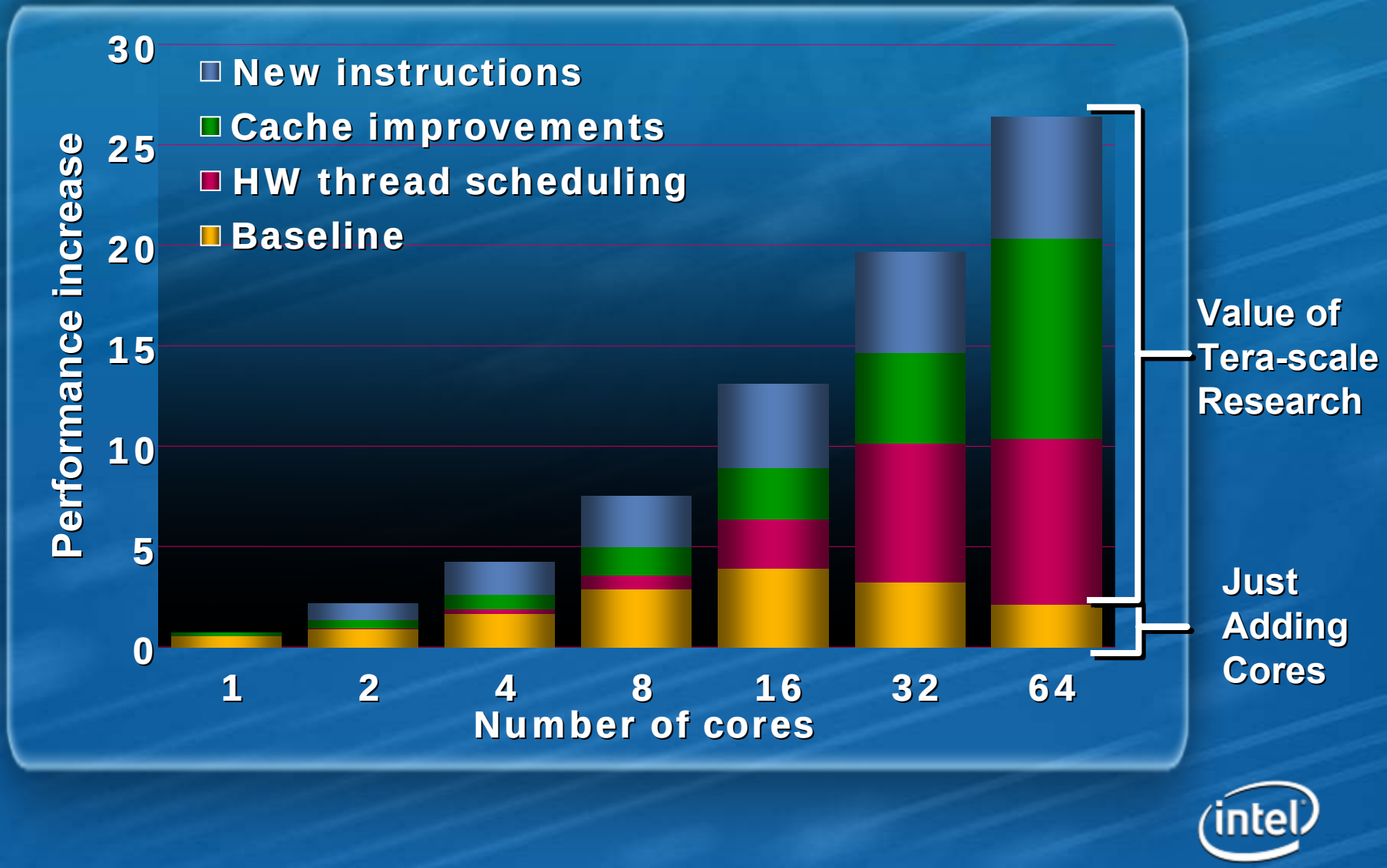
# Research Data Summary

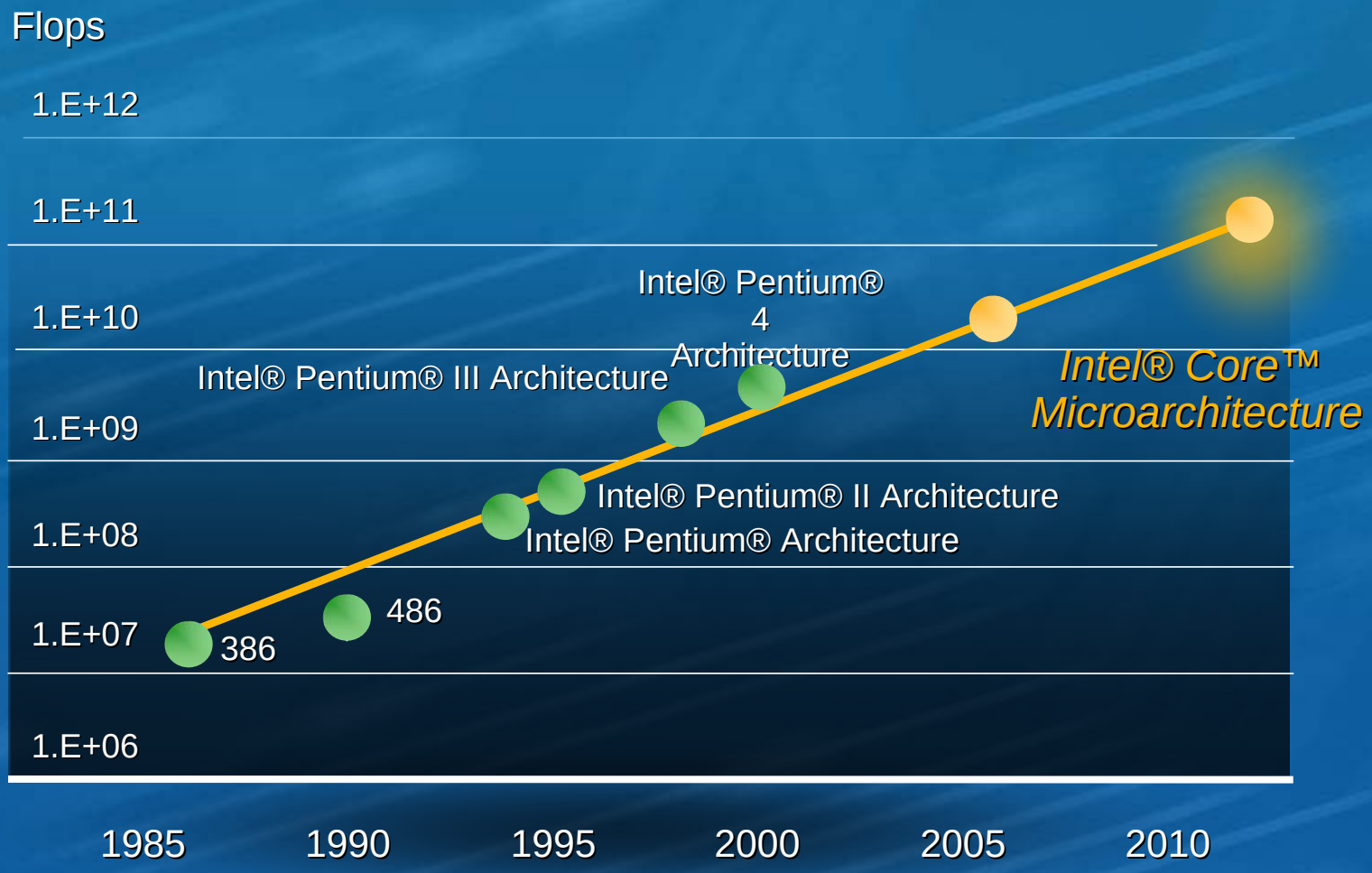
| Frequency | Voltage | Power | Bisection Bandwidth | Performance |
|---|---|---|---|---|
| **3.16 GHz** | **0.95 V** | **62W** | **1.62 Terabits/s** | **1.01 Teraflops** |
| 5.1 GHz | 1.2 V | 175W | 2.61 Terabits/s | 1.63 Teraflops |
| 5.7 GHz | 1.35 V | 265W | 2.92 Terabits/s | 1.81 Teraflops |

**1.01 Teraflops**
**62 Watts**

# More than the Cores



# Processor Performance

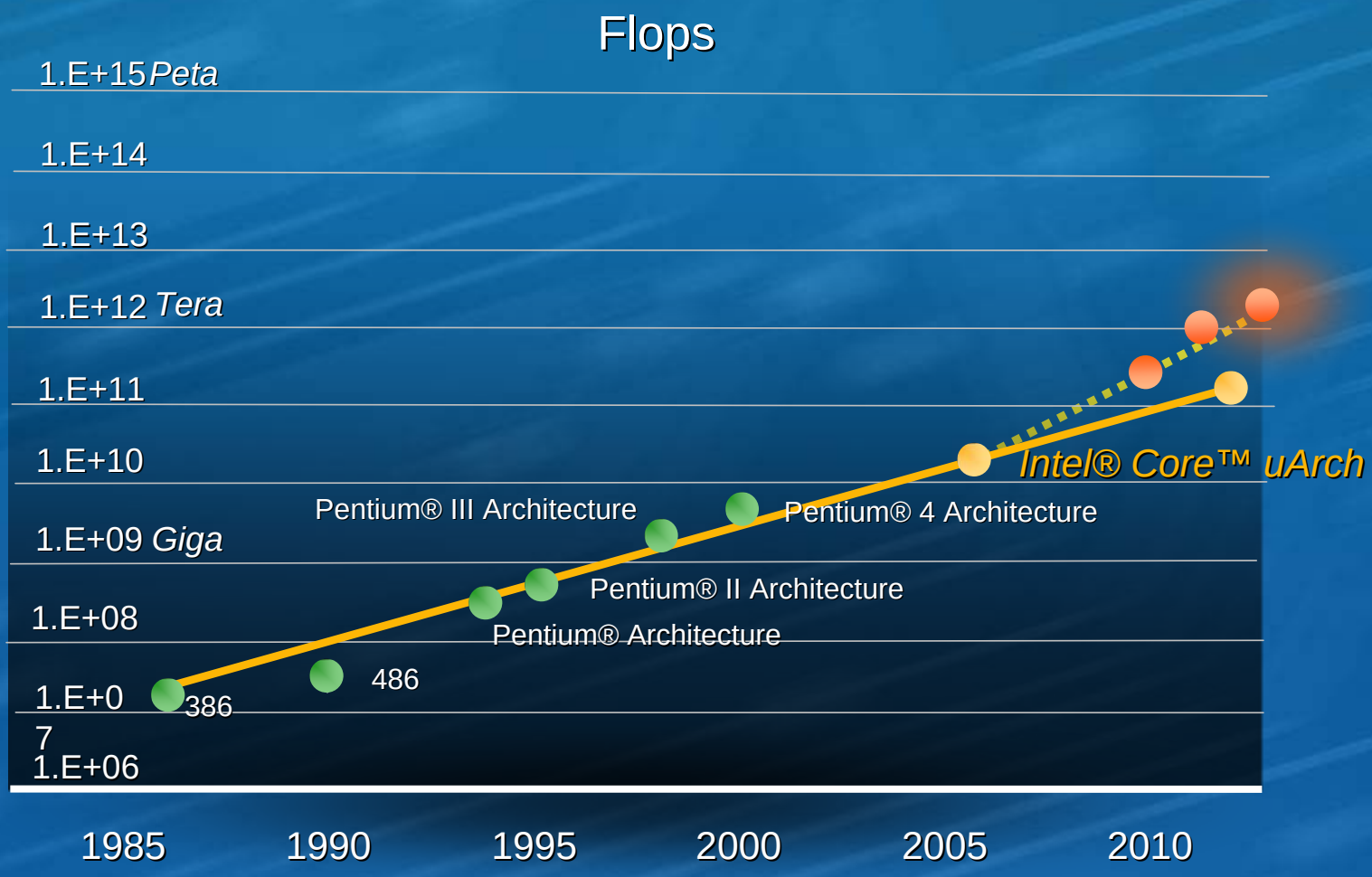



*Reaching Petascale with ~10,000 Processors in 2010**

Assuming approx. 100GF processors

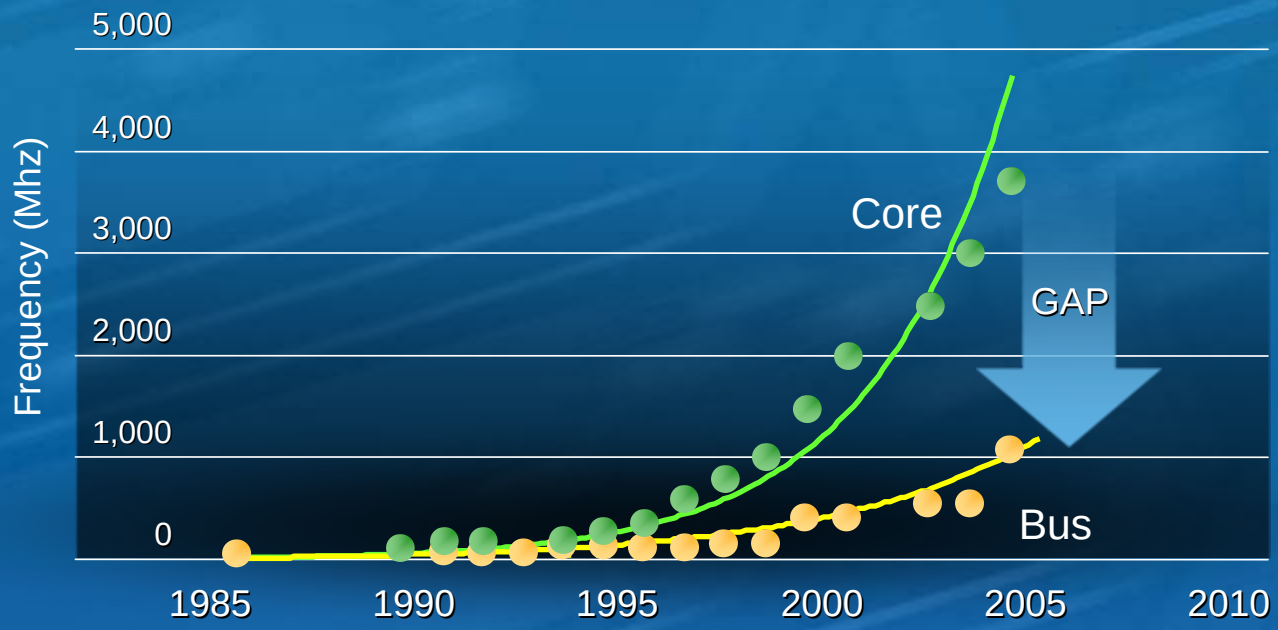
# Increasing Processor Performance

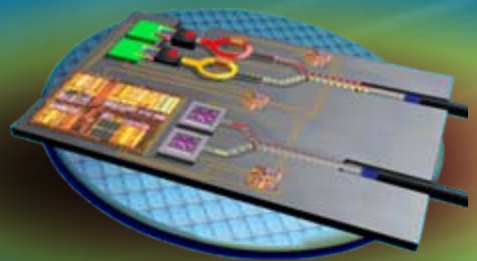
## *Through Multi-threaded Cores*




*Reaching Petascale with ~1,000 Processors*

# Increasing I/O Signaling Rate to Fill the Gap

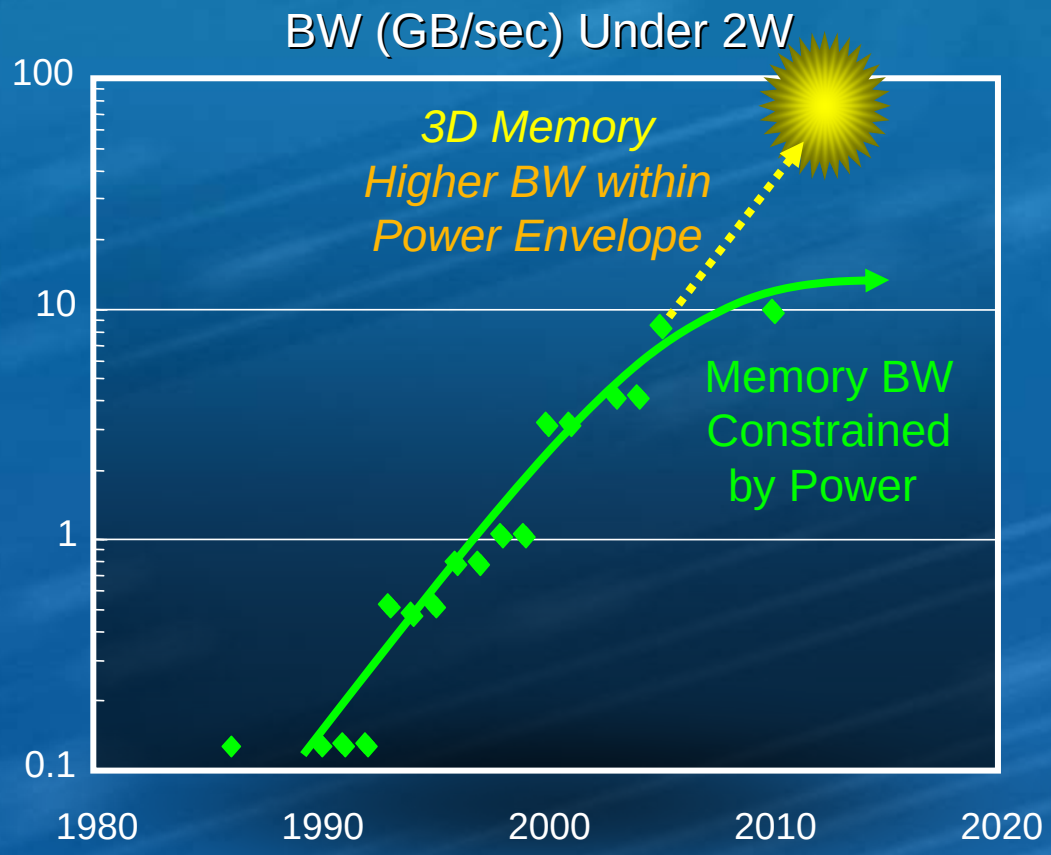


*Silicon Photonics*

Source: Intel

# Increasing Memory Bandwidth
## *to Keep Pace*

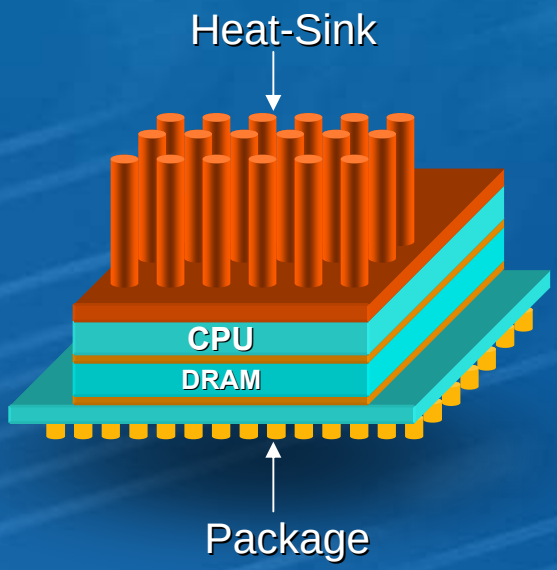



## *3D Memory Stacking*

*Power and IO Signals Go Through DRAM to CPU*

*Thin DRAM Die*

*Through DRAM Vias*




Source: Intel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Leap ahead™
HPC @ Intel